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Park

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[54] SEMICONDUCTOR MEMORY DEVICE

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[57] ABSTRACT

Semiconductor memory device which can support a DDR SDRAM latency mode like 2.5 for easy application to a high data rate memory, including a memory cell array having a plurality of memory cell regions for storing external data and forwarding the data on two lines by a decoded column address, a data path unit for forwarding the data from the memory cell array received through the two lines outwardly synchronous to an edge of internal clock, a controlling unit for controlling the data path unit entirely, a FIFO unit for controlling a forwarding order of the two data received from the data path unit, a latency pipeline controlling unit for providing an Enable signal for setting a data output enable interval at each of the control unit and the data path unit, a clock generating unit for providing the internal clock to the FIFO unit, the data path unit and the latency pipeline controlling unit for obtaining a desired band width, and a burst counter for providing a read signal having information on a burst length to the FIFO unit and the latency pipeline control unit.

10 Claims, 9 Drawing Sheets

